United States Patent [19]

Humphrey et al.

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[45] **Date of Patent: Jun. 12, 1990**

[54] **NETWORK COMMUNICATIONS ADAPTER WITH DUAL INTERLEAVED MEMORY BANKS SERVICING MULTIPLE PROCESSORS**

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[73] Assignee: **Network Systems Corporation**, Minneapolis, Minn.

[21] Appl. No.: **41,985**

[22] Filed: **Apr. 24, 1987**

[51] **Int. Cl.**[5] **G06F 13/00**; G06F 13/24; G06F 15/16

[52] **U.S. Cl.** **364/200**; 364/246.4; 364/243; 364/243.6; 364/231.4; 364/242.94; 364/242.95; 364/238.5; 364/240; 364/240.1; 364/270; 364/271.4; 370/85.1

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 370/85

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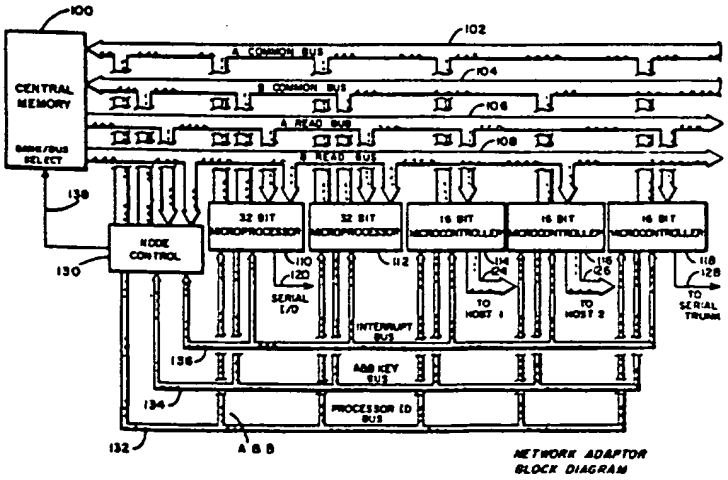
[57] **ABSTRACT**

A network communications adapter interconnects a plurality of digital computing resources for mutual data exchange in which a high performance, large capacity common memory is provided with a pair of external buses which allows multiple processors to store information in and read information from the common memory. The common memory is configured into two banks, each bank operating independently and concurrently under control of bus switching logic with separate address, control and data buses. The common memory typically provides 400 megabits per second of bandwidth to the multiple attached thirty-two and sixteen bit processors which may be coupled either to both buses simultaneously or individually to the two buses. The bus switching logic then allocates all of the available bandwidth to the individual processors coupled to the buses based upon a predetermined profile established at the time of system installation. Also included in the bus switch logic is circuitry for broadcasting a processor I.D., whereby only a particular processor assigned the same identifier will be afforded an access slot time during which communication over the dual bus structure can take place. One of the interconnected processors is designated as the node controller and it includes circuitry and software for implementing interprocessor interrupt handling and storage protection functions. Others of the plurality of processors coupled to the two memory buses provided input/output interfaces for host computers, digital peripheral devices, communications trunks or buses, or to wireless links for more remote communication.

4 Claims, 22 Drawing Sheets



42/3,K/38 (Item 38 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007534213 **Image available**
WPI Acc No: 1988-168145/198824
XRPX Acc No: N88-128505
High-speed digital data bus **for communication system - has minimum throughput penalty on** bus **and is** dynamically **re-** assignable **to accommodate changes in load pattern of message traffic**
Patent Assignee: NETWORK SYSTEMS CORP (NETW-N)
Inventor: DREWLO K G
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4748617	A	19880531	US 85811750	A	19851220	198824 B
JP 1073941	A	19890320	JP 87231994	A	19870916	198917

Priority Applications (No Type Date): US 85811750 A 19851220; JP 87231994 A 19870916
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4748617	A		54		

High-speed digital data bus **for communication system...**
...has minimum throughput penalty on bus **and is** dynamically **re-** assignable **to accommodate changes in load pattern of message traffic**

...Abstract (Basic): high speeds. The system includes several intelligent nodes termed DATA pipe adapters (RTM), which are **coupled** to a fibre optic **bus** .
...

...The adapters function as **interface devices** between the fibre optic **bus** and the I/O processors which are used to **couple** the user **devices** and networks to the adapters. A **synchronisation** pattern detector is provided in each of the nodes. Each of the nodes includes serial
...Title Terms: **BUS** ;
...International Patent Class (Additional): **G06F-013/00**
Manual Codes (EPI/S-X): **T01-H07** ...

United States Patent [19]

Drewlo

[11] **Patent Number: 4,748,617**

[45] **Date of Patent: May 31, 1988**

[54] **VERY HIGH-SPEED DIGITAL DATA BUS**

[75] Inventor: **Kenneth G. Drewlo, Maple Grove, Minn.**

[73] Assignee: **Network Systems Corporation, Minneapolis, Minn.**

[21] Appl. No.: **811,750**

[22] Filed: **Dec. 20, 1985**

[51] **Int. Cl.**[4] **H04J 3/02; G02F 1/00**

[52] **U.S. Cl.** **370/85; 370/94; 455/612**

[58] **Field of Search** 370/85, 110.1, 100, 370/4, 94, 96; 375/107, 117; 455/612; 340/825.5

[56] **References Cited**

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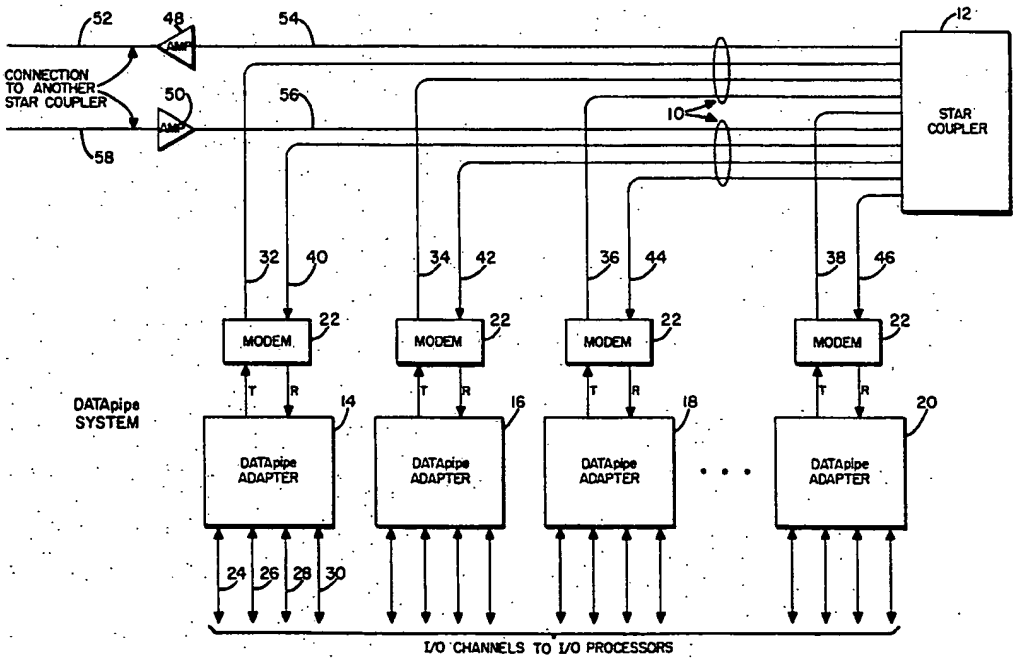
Primary Examiner—Douglas W. Olms
Assistant Examiner—Frank M. Scutch, III
Attorney, Agent, or Firm—Orrin M. Haugen; Thomas J. Nikolai; Frederick W. Niebuhr

[57] **ABSTRACT**

A time-division multiplexed, data communications system allowing multiple user devices, including super computer buses configured in a local network, and other existing network hierarchies to exchange digital data over extended distances at speeds heretofore unattainable. The system includes a plurality of intelligent nodes, termed "DATApipe TM adapters", which are coupled to a fiber optic bus. The DATApipe adapters function as interface devices between the fiber optic bus and the I/O processors which are used to couple the user devices and networks to the DATApipe adapters.

17 Claims, 16 Drawing Sheets



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Set     Items   Description
S1     498572   DIVID? OR DIVY? OR ALLOCAT? OR ALLOT? OR DIVVY? OR RATION?
S2    1203846   APPORTION? OR DESIGNAT? OR ASSIGN? OR EARMARK? OR DISPENS?
            OR SHARE?
S3     170710   METE? OR PARCEL?()OUT OR DOLE? OR DELEGAT? OR RELEGAT? OR -
            PRORAT? OR PRO()(RATA? OR RATE?)
S4     707435   DISTRIBUT? OR CORRELAT? OR COLLOCAT? OR CONSIGN? OR ROUTE?
S5    1339588   PARTITION? OR SEGMENT? OR PORTION? OR SECTION? OR SUBBUS? -
            OR SUB()(BUS OR BUSES)
S6     259164   DYNAMIC? OR ON(2W)FLY OR REALTIME? OR REAL()TIME? OR WHEN(-
            )NEEDED OR CHANGABL? OR CHANGEABL?
S7      89780   HOTSWAP? OR HOT()SWAP? OR AS()NEEDED? OR CASE(2W)CASE()BAS-
            IS? OR CUSTOMIZ? OR CUSTOMIS?
S8     573778   (CUSTOM? OR TAILOR?)()(MAKE? OR MAKING? OR MADE?) OR CONTI-
            NUOUS? OR CONSTANTLY?
S9     113068   BUS OR BUSSES
S10    113975   PCI? ? OR ISA? ? OR EISA? ? OR VLBUS? OR AGP? ? OR USB? ? -
            OR MCA? ? OR VESABUS? OR VESALOCAL?
S11    682456   CONNECTOR? OR PIN? ? OR CONDUCTOR? OR WIRE? OR (ELECTRIC? -
            OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(PATH? OR VIA? ?
             OR CONNECTION?) OR DATA()TRANSMITTER?
S12    133109   (ELECTRIC? OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(-
            TRACK? OR LANE? OR CHANNEL? OR PORT? OR INTERCONNECT?)
S13    226016   S1:S5(10N)S9:S12
S14    216631   ACCORDING? OR DEPENDING? OR PER OR ONE(2W)ONE OR CORRESPON-
            D?
S15    180664   MATCH? OR CONFORM? OR COINCID? OR CONSISTEN? OR SIMILAR? OR
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S16    126550   EQUAL? OR PROPORTION? OR CONTINGEN? OR HING? OR PREDICAT? -
            OR RELEGAT?
S17     83931   RELY? OR RELIAN? OR COMMENSURAT? OR EQUIVAL? OR COMPARABL?
            OR EQUIVAL?
S18     68076   COMPATIB? OR HOMOLOG? OR SYMMET? OR SYNONYM? OR HOMOGEN? OR
             EVENLY?
S19    189488   NUMBER? OR VOLUME? OR QUANTIT? OR AMOUNT? OR HOW()MANY
S20    157748   MAGNITUD? OR QUOTA? OR ASSEMBLAG? OR SIZE? OR TOTAL? OR AC-
            CUMULATION?
S21    188846   ABUNDAN? OR DIMENSION? OR WORKLOAD? OR BANDWIDTH? OR PLURA-
            L? OR MULTIP? OR MULTIT?
S22    218080   ATTACH? OR CONNECT? OR LINK? OR INSTALL? OR PLUG?()IN OR A-
            PPEND? OR CONFIGUR?
S23    142644   COUPL? OR AFFIX? OR HOOK?()UP OR NETWORKED? OR YOKE? OR IN-
            TERFAC?
S24    192739   DEVICE? OR HARDWARE? OR APPLIANC? OR APPARAT? OR ATTACHMEN-
            T? OR MODULE?
S25    148096   COMPONENT? OR PERIPHERAL? OR PDA? ? OR PALMPILOT? OR PALM(-
            )PILOT? OR ELECTRONIC()PC
S26      4485   (PORTABL? OR MOBIL? OR HANDHELD? OR HAND()HELD? OR ELECTRO-
            NIC? OR PALMTOP? OR PALM()TOP)()(UNIT? ? OR ORGANIZER?)
S27     21844   IC=G06F?
S28     38856   S13 AND S6:S8(7N)(S1:S5 OR S9:S12)
S29     21610   S28 AND S1:S8(7N)S14:S18(15N)S23:S26
S30      4593   S29 AND S1:S5(7N)S14:S18(7N)S19:S21(7N)S22:S23(7N)S24:S26
S31       470   S30 AND S1:S5(5N)S6:S8(5N)S9:S12(5N)S14:S18(5N)S19:S23(5N)-
            S24:S26
S32       141   S31 AND S27
S33       470   S31 AND S19:S21 AND S22:S23 AND S24:S26
S34       420   S33 AND S1:S18(5N)S19:S21(5N)S22:S23(5N)S24:S26
S35       213   S34 AND S1:S5(5N)S6:S8(5N)S9:S12
S36       276   S32 OR S35
S37     36642   AD=2003:2005
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S38 250 S36 NOT S37
S39 250 IDPAT (sorted in duplicate/non-duplicate order)
File 348:EUROPEAN PATENTS 1978-2005/Sep W04
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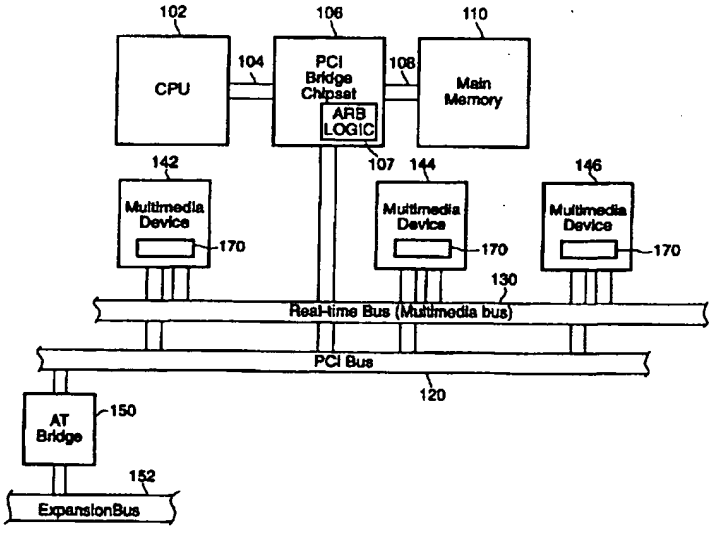
(54) Title: A COMPUTER SYSTEM HAVING A MULTIMEDIA BUS AND COMPRISING A CENTRALIZED I/O PROCESSOR WHICH PERFORMS INTELLIGENT DATA TRANSFERS



(57) Abstract

A computer system optimized for real-time applications which provides increased performance over current computer architectures. The system includes a standard local system bus or expansion bus, such as the PCI bus, and also includes a dedicated real-time bus or multimedia bus. Various multimedia devices are coupled to one or more of the expansion bus and/or the multimedia bus. The computer system includes a dedicated or centralized I/O processor coupled to one or more of the expansion bus and/or the multimedia bus which operates to direct or pull stream information through the system. The centralized I/O processor comprises a memory for storing data rate, data periodicity, data source, and data destination information for said multimedia devices. The computer system of the present invention thus provides much greater performance for real-time applications than prior systems.

39/3,K/48 (Item 48 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00909785
A COMPUTER SYSTEM HAVING A MULTIMEDIA BUS AND COMPRISING A CENTRALIZED I/O PROCESSOR WHICH PERFORMS INTELLIGENT DATA TRANSFERS
EIN AUS EINEM MULTIMEDIA-BUS UND EINEM ZENTRALEN EIN/AUSGABEPROZESSOR BESTEHENDES RECHNERSYSTEM, DAS INTELLIGENTE DATENUBERTRAGUNGEN AUSFUHRT
SYSTEME D'ORDINATEUR DOTE D'UN BUS MULTIMEDIA ET COMPRENANT UN PROCESSEUR E/S CENTRALISE QUI EFFECTUE DES TRANSFERTS DE DONNEES INTELLIGENTS
PATENT ASSIGNEE:
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INVENTOR:
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PATENT (CC, No, Kind, Date): EP 898749 A1 990303 (Basic)
EP 898749 B1 010926
WO 9744740 971127
APPLICATION (CC, No, Date): EP 97926565 970516; WO 97US8363 970516
PRIORITY (CC, No, Date): US 650938 960517
DESIGNATED STATES: DE; ES; GB
INTERNATIONAL PATENT CLASS: **G06F-013/40** ; **G06F-013/12**
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200139	399
CLAIMS B	(German)	200139	346
CLAIMS B	(French)	200139	460
SPEC B	(English)	200139	16255
Total word count - document A			0
Total word count - document B			17460
Total word count - documents A + B			17460

PATENT ASSIGNEE:
Advanced Micro **Devices** , Inc...
INTERNATIONAL PATENT CLASS: **G06F-013/40** ...

... **G06F-013/12**

...SPECIFICATION devices 142-146 may be comprised on a modular expansion card 400 including PCI bus **connector** 402 and multimedia bus **connector** 404. This **configuration** allows for more modular and upgradeable expansion options in the computer system. This also provides...

...multimedia devices include PCI bus connector 402 but do not include a real-time bus **connector** 404. These prior art multimedia **devices** are simply inserted into a respective PCI expansion slot 122, and the **corresponding real - time connector** slot 132 is not used for that respective PCI expansion slot 122. Thus, the computer...

...receive new expansion cards 400 according to the present invention which

include both a PCI **bus** **connector** 402 and real-time **bus** **connector** 404.

Figure 6 - Alternate Embodiment

Referring now to Figure 6, an alternate embodiment of the...

...of Figure 1 is shown. In the embodiment of Figure 6, chipset logic 106A is **connected** to both the local expansion bus 120 as well as real-time **bus** 130A. In this embodiment, the multimedia **bus** 130A may be different from the multimedia bus 130 shown in Figure 1 to accommodate CPU accesses through the chipset logic 106A to the real- **time** **bus** 130A, and also to accommodate **peripheral** **device** accesses through the real- **time** **bus** 130A and chipset logic 106A to main memory 110. Also, multimedia **devices** 142 - 146 which are **coupled** to the PCI **bus** 120 and the **real - time** **bus** 130A in Figure 6 may be different from the multimedia **devices** 142 - 146 in Figure I to accommodate accesses through the real- **time** **bus** 130A to main memory 110.

Thus, in this embodiment, the chipset logic 106A can communicate directly to the PCI bus 120, and can also communicate directly with the real- **time** or multimedia **bus** 130. This facilitates operation of the CPU 102 communicating with the multimedia **devices** 142 - 146 through both the PCI bus 120 and the multimedia bus 130A. In addition, one or more of the multimedia **devices** 142-146 can use the multimedia bus 130A to **interface** through the chipset logic 106A to the main memory 110 as desired.

Figure 7 - Computer...

...system of Figure 7 includes a separate control channel 502 in addition to the PCI **bus** 120 and the **real - time** or multimedia **bus** 130. As described below, multimedia **devices** use the multimedia bus 130 for high speed data transfers and use the dedicated control...

...convenience.

As shown, the computer system includes a central processing unit (CPU) 102 which is **coupled** through a CPU local bus 104 to a host/PCI/cache bridge or chipset 106. The chipset 106 includes various bridge logic, **peripheral** logic and arbitration logic 107, as described above with reference to Figure I. The bridge or chipset 106 **couples** through a memory bus 108 to main memory 110. The main memory 110 is preferably...

...types of memory, as desired. The chipset logic 106 preferably includes a memory controller for **interfacing** to the main memory 110.

The host/PCI/cache bridge or chipset 106 **interfaces** to a local expansion bus or system bus 120. In the preferred embodiment, the local expansion bus 120 is the **peripheral** **component** interconnect (PCI) bus 120. However, it is noted that other local buses may be used, such as the VESA (Video Electronics Standards Association) VL bus. Various types of **devices** may be **connected** to the PCI bus 120. Expansion bus bridge logic 150 and an expansion bus 152 may also be **coupled** to the PCI bus 120, as described above.

The computer system shown in Figure 7 includes a real-time **bus** , also referred to as a multimedia **bus** 130. The multimedia bus 130 preferably includes a 32 or 64 bit data **path** and in this embodiment does not include address and control **portions** . The computer system shown in Figure 7 further includes a dedicated control channel 502 separate...

...be used to transfer interrupt, synchronization, and status commands and information.

One or more multimedia **devices** 142A, 144A, and 146A are **coupled** to each of the PCI bus 120 and the multimedia bus 130. The multimedia **devices** 142A-146A each include bus **interface** circuitry 512 which

includes standard PCI **interface** circuitry for communicating on the PCI bus 120, **interface** logic for **interfacing** to the multimedia bus 130, and control channel **interface** logic for **interfacing** to the control channel 502. The multimedia **devices** 142A - 146A use the multimedia bus 130 to communicate data between the respective **devices** and use the control channel 502 for addressing and control of the multimedia bus 130.

The multimedia **devices** 142A-146A may be any of various types of input/output **devices** ; including multimedia **devices** and communication **devices** , as described above. The multimedia **devices** 142A-146A are preferably similar to the multimedia **devices** 142 - 146 described above, except that the **interface** logic 512 in the multimedia **devices** 142A-146A each include control channel **interface** logic, as described below. As described above, the multimedia **devices** 142A - 146A may comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards, network **interface** cards, SCSI adapters for **interfacing** to various input/output **devices** , such as CD-ROMS and tape drives, or other **devices** as desired.

Thus, the multimedia **devices** 142A - 146A communicate with each other via the PCI bus 120 and also communicate with...

...110 via the PCI bus 120, as is well known in the art. The multimedia **devices** 142A - 146A also communicate data between each other using the real-time **bus** or multimedia **bus** 130. When the multimedia **devices** 142A - 146A communicate using the real- **time** **bus** 130, the **devices** use the control channel 502 for addressing, control, status and handshaking signals. Thus the **devices** 142A - 146A do not utilize any PCI bus cycles when communicating over the multimedia bus 130.

In the embodiment of Figure 7, arbitration logic 504 is **coupled** to the control channel 502 and performs arbitration for the **devices** 142A - 146A on the bus 130. Alternatively, arbitration logic 504 is incorporated into the PCI Bridge Chipset 106. In these embodiments, the multimedia **devices** 142A - 146A provide request signals on the control channel 502 to the arbitration logic 504, and the arbitration logic 504 grants bus access according to a desired arbitration method.

Multimedia **devices**

Referring now to Figure 8, a block diagram is shown illustrating one of the multimedia **devices** 142A-146A, such as multimedia **device** 142A. As shown, the multimedia **device** 142A includes **interface** logic 512 comprising PCI **interface** circuitry 522 for communicating on the PCI bus 120, multimedia bus **interface** logic 524 for **interfacing** to the multimedia bus 130, and also including control channel **interface** logic 526 for **interfacing** to the control channel 502. The multimedia **device** 142A also may include a digital signal processor (DSP) 210 or other **hardware** circuitry for implementing a multimedia or communications function. Each of the multimedia devices 142A - 146A...

...use the multimedia or real-time bus 130 only for high speed data transfers of **real** -time stream data information. In one embodiment the multimedia bus 130 transfers only **periodic** stream data, i.e., data streams which require **periodic** transfers for multimedia or communication purposes, as described above. Examples of periodic data include audio...

...bus 130 includes primarily data lines, such as a 32 bit or 64 bit data **path** , and does not include address or arbitration **portions** . In this embodiment of the invention, each of the multimedia **devices** 142A - 146A uses the ...502 for addressing and control for transfers on the multimedia bus 130. Thus the multimedia **devices** 142A - 146A use the

multimedia or real- **time** **bus** 130 only for high speed data transfers. Thus, in this embodiment, the multimedia bus **interface** logic 524 includes only data signal pins for **interfacing** to the data lines comprising the multimedia bus 130. Also, PCI bus **bandwidth** is not affected by multimedia bus transfers.

Figure 9A - Flowchart Diagram
Referring now to Figure...

...of a multimedia data transfer according to the embodiment of Figure 7. When a multimedia **device** 142A desires to perform a transfer, in step 542 the control channel **interface** logic 526 in the transferring **device** transfers control information on the control channel 502 to set up the transfer. This involves...

...and status information regarding the length of the transfer, among other status information. The transferring **device** provides the control information to the respective destination **device** .

Once the transfer has been set up on the control channel 502 in step 542, then in step 544 the transferring **device** performs the data transfer on the multimedia bus 130 to the receiving or target **device** . During the entire transfer in steps 542 and 544, the PCI bus 120 is free ...

...illustrating a data transfer method optimized for periodic transfers is shown. This method minimizes the **amount** of addressing and control handshaking and increases performance as described above by essentially using preset...

...multimedia bus 130, in step 552 the control channel interface logic 526 in the multimedia **device** 142 first transfers control information on the control channel 502 to the arbitration logic 504...

...transfer, information regarding the length of the transfer and other status information.

Once the requesting **device** has received control of the bus 130. in step 554 the transferring **device** provides a periodic data transfer request to the target **device** . This periodic data transfer request may be transferred over the control channel 502 or the...

...130. As described above, the periodic data transfer request comprises a request for the multimedia **device** acting as the transmitter to periodically transfer a data stream to the receiving **device** at a predetermined frequency without requiring each individual transfer to be set up with control...

...periodic transfers as well as any real-time constraint information.

In response to the transferring **device** transferring the **periodic** transfer request in step 554, the receiving **device** uses the received information to determine if it can guarantee availability at the requested time frequency to receive the data. If the receiving **device** can guarantee availability for receiving this periodic data, then the receiving **device** preferably performs a handshake to indicate that the periodic data transfers can be performed. The receiving **device** also preferably **configures** one or more timers or counters at the specified frequency to indicate when the receiving **device** should enable its buffers and transceivers to receive the periodic data on the bus 130...

...device has indicated availability for the periodic transfer. Thus, when the receiving device receives the **periodic** data transfer request in step 554, the receiving device determines if the receiving device can...

...If the receiving device cannot guarantee availability at the frequency or period specified by the **periodic** data transfer request, then the receiving **device** indicates that it is not available for periodic data transfers. In this case, in step 562 the transmitting multimedia **device** sets the periodic transfer flag to no and in step 564 performs a single transfer...

...requires that step 552 be performed to transfer control and addressing information to the receiving **device** to set up the transfer.

If the receiving **device** indicates availability for the periodic data transfer in step 556, then in step 558 the transmitting multimedia **device** sets the periodic transfer flag to yes and in step 560 the transferring **device** begins the first of a **plurality** of periodic transfers at the frequency or period specified in the periodic data transfer request in step 554. If the transferring **device** has indicated a desire to transfer periodic data streams on the multimedia bus 130, and the receiving **device** has indicated availability to perform the transfers, then the transferring **device** performs periodic transfers of data streams to the receiving **device** . In this instance, the receiving **device** has indicated that it can guarantee availability at the times required by the transmitting **device** . Thus the receiving is available to receive each transfer of periodic data.

Figure 10 - Multimedia Channels

Referring now to Figure 10, a computer system is shown which includes a **plurality** of individual multimedia channels for two or more of video data, audio data, and communication...

...convenience.

As shown, the computer system includes a central processing unit (CPU) 102 which is **coupled** through a CPU local bus 104 to a host/PCI/cache bridge or chipset 106. The chipset 106 includes various bridge logic, **peripheral** logic and arbitration logic 107, as described above with reference to Figure 1. The bridge or chipset 106 **couples** through a memory bus 108 to main memory 110. The main memory 110 is preferably...

...types of memory, as desired. The chipset logic 106 preferably includes a memory controller for **interfacing** to the main memory 110.

The host/PCI/cache bridge or chipset 106 **interfaces** to a local expansion bus or system bus 120. In the preferred embodiment, the local expansion bus 120 is the **peripheral** **component** interconnect (PCI) bus 120. However, it is noted that other local buses may be used. Various types of **devices** may be **connected** to the PCI bus 120. Expansion bus bridge logic 150 and an expansion bus 152 may also be **coupled** to the PCI bus 120, as described above.

The computer system shown in Figure 10 includes a **plurality** of real-**time** **data** **channels** , including a video channel 602, an audio channel 604, and a communications channel 606. In...

...may each have individual addressing and control portions or may use the addressing and control **portions** of the expansion **bus** 120.

One or more multimedia **devices** or multimedia **devices** 142B, 144B, and 146B are **coupled** to each of the PCI bus 120 and to each of the data channels 602 - 606. The multimedia **devices** 142B - 146B preferably **multiplex** data onto the respective channels for reduced pinout requirements. The multimedia **devices** 142B - 146B each include bus **interface** circuitry 612 which includes standard PCI **interface** circuitry for communicating on the PCI bus 120, and **interface** logic for **interfacing** to each of the channels 602 - 606. The multimedia **devices**

142B-146B use the respective channels 602 - 606 to communicate data of the respective data type between the respective **devices** .

As described above, the multimedia **devices** 142B - 146B may be any of various types of input/output **devices** , including multimedia **devices** and communication **devices** , as described above. The multimedia **devices** 142B - 146B are preferably similar to the multimedia **devices** 142 - 146 described above, except that the **interface** logic 612 in each of the multimedia **devices** 142B - 146B includes channel **interface** logic for each data channel 602 - 606. As described above, the multimedia **devices** 142B - 146B may comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards, network **interface** cards, SCSI adapters for **interfacing** to various input/output **devices** , such as CD-ROMS and tape drives, or other **devices** as desired.

Thus, the multimedia **devices** 142B - 146B communicate with each other via the PCI bus 120 and also communicate with...

...110 via the PCI bus 120, as is well known in the art. The multimedia **devices** 142B - 146B also communicate data between each other using the data channels 602 - 606:

The multimedia **devices** 142B - 146B use each of these channels 602 - 606 for high speed data transfers. The multimedia **devices** 142B - 146B use either the PCI bus 120 or a dedicated control channel (not shown...

...channel (not shown), as described above with reference to Figure 7, arbitration logic 614 is **coupled** to each of the data channels 602 - 606 and the control channel and performs arbitration for the **devices** 142B - 146B on the channels 602 - 606. In this embodiment, the multimedia **devices** 142B - 146B provide request signals on the control channel to the arbitration logic 614, and...

...logic 614 grants channel access according to a desired arbitration method.

Figure 11 - Multimedia Bus **Interface** with Timeslotting Logic

Referring again to Figures 1 and 7, in one embodiment the multimedia...

...time sliced wherein time slices or time slots are allocated in proportion to the required **bandwidth** . In this embodiment, the multimedia **devices** , such as the multimedia **devices** 142 shown in Figure 2 or 142A shown in Figure 8 include time slotting logic. Referring now to Figure 11, logic **components** of a multimedia bus **interface** 174 comprised in the multimedia **devices** in this embodiment are shown. Multimedia bus **interface** logic 174A shown in Figure 11 is preferably comprised in each of the multimedia **devices** comprised in the computer system, such as the multimedia **devices** 142-146 shown in Figure 1 or the multimedia **devices** 142A-146A shown in Figure 7. As shown, each multimedia bus **interface** 174A in the **device** includes bus transceivers and buffers 642 for **interfacing** to the respective multimedia bus 130.

The multimedia bus **interface** 174A also includes timeslotting logic 644 for controlling access of the respective multimedia **device** to the multimedia bus 130. The timeslotting logic 644 preferably uses one or more timers and counters 646 for determining respective timeslot. The multimedia bus **interface** logic 174A also includes programmable timeslot registers which are programmed by a central agent, such...

...bus. In one embodiment. the CPU 102 programs a timeslot into each of the multimedia **devices** at startup or boot time, thus providing a static allocation of timeslots. Alternatively, software executing on the CPU 102 dynamically programs timeslots in each of the multimedia **devices** dependent upon real-time processes and applications occurring in the

computer system. The timeslotting logic...

...646 and the programmable timeslot registers 648 storing the respective timeslot allocated to the respective **device** . The multimedia **bus interface** logic 174A further includes multimedia bus monitoring logic 650 for monitoring conditions on the bus...

...includes collision detection logic 652 for determining when a bus transfer from the respective multimedia **device** has inadvertently collided with another **devices** transfer. The multimedia bus monitoring logic 650 preferably insures that the multimedia bus 130 is...

...In one embodiment, as shown in Figure 12A, the time slices are each a constant **size** and a **number** of the equal **sized** time slots are allocated to respective data streams in proportion to the required band width...

...device. In this embodiment, arbitration for the multimedia bus is not required. Rather, a multimedia **device** programmed as a transmitter of video data monitors the bus and includes controller circuitry which begins transmitting the video data when the **device** 's respective time slot occurs. A corresponding **device** programmed as a receiver of said data also knows that the current time slot is...

...video time slot and monitors the bus to receive the data.
In this embodiment, the **interface** circuitry of each of the multimedia **devices** are programmed at boot time for a static allocation of time slots. Alternatively, the interface...

...corresponding data transfer bandwidth requirements. For example, the CPU may program each of the multimedia **devices** with a respective time slot at power-on. Alternatively, if the mix of real-time processes change, the CPU may **dynamically** or heuristically **allocate** time slots based on **bandwidth** requirements.

Figure 13 - Centralized I/O Processor
Referring now to Figure 13, an alternate embodiment...

...that the system shown in Figure 13 includes a dedicated multimedia I/O processor 702 **coupled** to the multimedia bus 130 which controls operations on the multimedia bus 130. The I...

...and coordinates all transfers within the system. Thus, the multimedia I/O processor 702 creates **connections** between two or more **devices** , sets up transfers between **devices** , and (optionally) executes the transfer. The centralized multimedia I/O processor 702 of the present...

...on a standard PCI bus 120. Alternatively, the centralized multimedia I/O processor 702 may **couple** to both the expansion bus 120 and the multimedia bus 130 and control operations on...

...shown in Figure 13 is shown. As shown, the multimedia I/O processor includes a **plurality** of data bus registers and/or a data bus memory which stores information regarding the data rates of each the **devices** , the data periodicity of each of the **devices** , and the respective data sources and destination **devices** comprised in the system. The multimedia I/O **device** 702 also includes data transfer control logic 714 which is **coupled** to the data bus registers and controls transfers on the multimedia bus 130. The multimedia...

...to use different byte channels simultaneously. In this embodiment, the multimedia bus 130 includes a **plurality** of data channels, preferably data byte lanes or channels, which may be used by different multimedia **devices** concurrently. Thus, a first data stream is transferred on a first one or more data...

...transferred on a second one or more data byte channels. Thus, where a first multimedia **device** 142 generates a first data stream and a second multimedia **device** 144 generates a second data stream, the byte slicing logic 716 assigns the first data stream to a first one or more data byte channels and **assigns** the second data stream to a second one or more **data** byte **channels** . In this case, the first multimedia **device** 142 generates the first data stream on the first one or more data byte channels substantially concurrently with the second multimedia **device** 144 generating the second data stream on the second one or more data byte channels.

Thus the byte sliced multimedia bus allows different **peripherals** to **share** the **bus** simultaneously. The byte slicing logic 716 in the centralized multimedia I/O processor 702 thus may assign one data stream to a subset of the **total** byte lanes on the multimedia bus 130, and fill the unused byte lanes with another...

...for storing data rate, data periodicity, data source, and data destination information for said multimedia **devices** , and the input/output processor 702 operates to selectively and dynamically **assign** data streams on selected ones of the **data** byte **channels** comprising the respective multimedia bus 130 and/or expansion bus 120 using the data rate, data periodicity, data source, and data destination information for said multimedia **devices** .

In this embodiment where a **plurality** of multimedia **devices** are **coupled** to the multimedia bus 130 and/or to the expansion bus 120, and wherein each of the multimedia **devices** perform operations on the multimedia bus 130 and/or the expansion bus 120, the byte slicing logic 716 operates to selectively and/or dynamically **assign** data streams on selected ones of the **data** byte **channels** comprising the respective bus.

It is noted that the byte slicing logic 716 may be...

...computer system comprises a multimedia bus 130 and/or an expansion bus 120 including a **plurality** of data byte channels for transmitting data, and a **plurality** of multimedia **devices** are **coupled** to the multimedia bus, wherein each of said multimedia **devices** perform operations on said multimedia bus130 and/or expansion bus 120. As shown, in step 722, a first multimedia **device** generates a signal indicating a transfer of a first stream of data. In step 724, a second multimedia **device** generates a signal indicating a transfer of a second stream of data. In step 726...

...of the respective bus, i.e., either the multimedia bus 130 and/or the expansion **bus** 120. In step 728 the byte slicing logic 716 **assigns** the second stream of data to a second one or more data byte channels of...

...of Figure 1. However, the computer system of Figure 15 includes a multimedia memory 160 **coupled** to each of the PCI **bus** 120 and to the **real - time bus** 130. In the following description, elements which are preferably identical to elements previously described include...

...convenience.

As shown, the computer system includes a central processing unit (CPU) 102 which is **coupled** through a CPU local bus 104 to a host/PCI/cache bridge or chipset 106B...

...the Triton chipset available from Intel Corporation, including certain arbiter modifications to accommodate the real- **time** **bus** 130 and the multimedia memory 160 of the present invention. A second level or L2 cache memory (not shown) may be **coupled** to a cache controller in the chipset. as desired. The bridge or chipset 106B **couples** through a memory bus 108 to main memory 110. The main memory 110 is preferably...

...types of memory, as desired.

The chipset logic 106B preferably includes a memory controller for **interfacing** to the main memory 110 and also includes the arbitration logic 107B. The chipset logic 106B preferably includes other various **peripherals** , as described above with reference to figure 1.

The host/PCI/cache bridge or chipset 106B **interfaces** to a local expansion bus 120. In the preferred embodiment, the local expansion bus 120 is the **peripheral** **component** interconnect (PCI) bus 120. However, it is noted that other local buses may be used, such as the VESA (Video Electronics Standards Association) VL bus. Various types of **devices** may be **connected** to the PCI bus 120.

The computer system shown in Figure 15 also includes a real-time **bus** , also referred to as a multimedia **bus** 130. The **real - time** **bus** 130 preferably includes a 32 or 64 bit data path and may also include address ...

...1 or the real-time bus 130A shown in Figure 1. Alternatively, the real-time **bus** 130 includes various address and control signals for accessing the multimedia memory 160.

Multimedia memory 160 is **coupled** to each of the PCI **bus** 120 and the **real - time** **bus** 130. In the embodiment of Figure 15, the multimedia memory 160 is preferably dual ported memory. In this embodiment, a first port of the memory 160 **couples** to the PCI bus 120. The second port of the multimedia memory 160 **couples** to the real- **time** **bus** 130. The multimedia memory 160 preferably comprises high speed dual ported VRAM (video random access...

...from Intel Corporation, which is hereby incorporated by reference.

In the preferred embodiment, the real- **time** **bus** 130 includes only a 32 bit or 64 bit data path and does not include address or arbitration portions. In one embodiment, **devices** use the **PCI** **bus** 120 for arbitration, addressing and setup, and **devices** use the multimedia or real- **time** **bus** 130 for high speed data transfers between each other and also to/from the multimedia memory 160. Thus, in one embodiment, **devices** use the PCI bus 120 to provide addressing and control signals to the multimedia memory 160 and use the multimedia or real- **time** **bus** 130 for high speed data transfers to and from the multimedia memory 160.

One or more multimedia **devices** 142C, 144C, and 146C are **coupled** to each of the PCI **bus** 120 and the **real - time** **bus** 130. The multimedia **devices** 142C - 146C include standard PCI **interface** circuitry for communicating on the PCI bus 120. The multimedia **devices** 142C - 146C also include **interfaces** to the real- **time** **bus** 130. The multimedia **devices** 142C - 146C use the real- **time** **bus** 130 to communicate data between the respective **devices** . As described above, one or more of the multimedia **devices** 142C - 146C may be comprised on modular expansion cards adapted for insertion into respective slots of each of the real-time **bus** 130 and **PCI** **bus** 120. One or more of the multimedia **devices** 142C - 146C may be implemented directly on the motherboard or on a custom circuit card plugged into the motherboard.

In one embodiment, arbitration logic 151 is **coupled** to the real- **time** **bus** 130 and performs arbitration for the devices 142C - 146C on the

bus 130. In this embodiment, the multimedia **devices** 142C - 146C provide request signals on the real- **time** **bus** 130, and the arbitration logic 151 grants bus access **according** to a desired arbitration method. Alternatively, the arbitration logic 151 is not included, and the multimedia **devices** 142C - 146C use the PCI **bus** arbitration to gain control of the **real - time** **bus** 130.

The multimedia **devices** 142C - 146C may be any of various types of input/output **devices** , including multimedia **devices** and communication **devices** . For example, the multimedia **devices** 142C - 146C may comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards. network **interface** cards, SCSI adapters for **interfacing** to various input/output **devices** , such as CD-ROMs and tape drives, or other **devices** as desired.

Thus, the multimedia **devices** 142C - 146C communicate with each other via the PCI bus 120 and communicate with the...

...110 via the PCI bus 120, as is well known in the art. The multimedia **devices** 142C - 146C also communicate data between each other and the multimedia memory 160 using the real-time **bus** or multimedia **bus** 130. When the multimedia **devices** 142C - 146C communicate using the real-**time** **bus** 130, the **devices** are not required to obtain PCI bus mastership and they do not consume PCI bus cycles. In one embodiment, the multimedia **devices** 142C - 146C communicate with the multimedia memory 160 using either or both of the real-time **bus** 130 and the **PCI** **bus** 120.

Expansion bus bridge logic (not shown) may also be **coupled** to the PCI bus 120. The expansion bus bridge logic **interfaces** to a secondary expansion bus (also not shown). The expansion bus may be any of...

...bus, the extended industry standard architecture (EISA) bus, or the microchannel architecture (MCA) bus. Various **devices** may be **coupled** to the expansion bus, such as expansion bus memory or a modem (both not shown).

In the embodiment of Figure 15, each of the multimedia **devices** 142C - 146C include PCI **interface** logic for **coupling** to the PCI bus 120 and also include real-time bus interface logic for **interfacing** to the **real - time** **bus** 130. Each of the multimedia **devices** 142C - 146C also include arbitration logic for gaining control of the real- **time** **bus** 130 and further include logic which gains access to the multimedia memory 160. Thus, each of the multimedia **devices** 142C - 146C can gain control of the real- **time** **bus** 130 and access the multimedia memory 160 to retrieve desired code and data.

In the...

...memory space.

In the embodiment shown in Figure 15, one or more of the multimedia **devices** 142C - 146C includes at least one DSP engine 210 which preferably performs a multimedia or...

...The DSP engine 210 may also be programmed to perform communication functions, such as ISDN **connectivity** or modem functionality, as desired. In another embodiment, the DSP engine is not a general purpose DSP engine but is instead a **device** that is optimized for the performance of one or more multimedia or communications functions.

In...

...to the multimedia memory 160 contemporaneously with operations performed by the one or more multimedia **devices** 142C - 146C. In one embodiment, the multimedia memory 160 is partitioned into two or more...

...first address space or buffer in the multimedia memory 160 while one of the multimedia **devices** 142C - 146C accesses commands and data from the other address space or buffer.

As mentioned...

...available to store non-multimedia data as needed. In this embodiment, each of the multimedia **devices** 142C - 146C and CPU 102 must also arbitrate for access to the multimedia memory 160. The multimedia **devices** 142C - 146C preferably have priority access to the multimedia memory 160. in one embodiment, a multimedia **device** simply writes one or more bits to a register in the arbitration logic 107B in...

...data through the PCI bus 120 directly to the multimedia memory 160, and the multimedia **devices** 142C - 146C access commands and data from the multimedia memory 160 through the multimedia bus...

...information regarding the multimedia data, including the beginning address of the data, the length or **number** of bytes of the data, as well as other information. Alternatively, the CPU 102 provides...

...based on a desired priority scheme and the available resources. Thus, the video and audio **components** of a multimedia presentation may receive a higher priority than a telephony application that can...commands reside. The pointer information includes the beginning address of the data, the length or **number** of bytes of the data, as well as other information. In step 510 the DMA...

...or retrieved from main memory 110, in step 512 one or more of the multimedia **devices** 142C-146C read the commands and data from the multimedia memory 160 and in step 514 perform the necessary graphics and audio processing functions. The respective multimedia **device** 142C - 146C then generates the appropriate video and audio signals to the video and audio...

...memory 160 is partitioned into separate address spaces for commands and data, and the multimedia **device** retrieves commands from a first address space and retrieves data from a second address space...

...order to minimize CPU accesses to the multimedia memory 160. This ensures that the multimedia **devices** 142C - 146C have full access to the multimedia memory 160 for real-time processing. Further, the multimedia **devices** 142C - 146C retrieve commands and data from the main memory 110 only when necessary, and the multimedia **devices** 142C - 146C are not "locked out" of the multimedia memory 160 due to CPU writes...

...CPU 102 writes to one address space or buffer while the one or more multimedia **devices** 142C - 146C accesses commands and data from the other address space or buffer. This ensures that the multimedia **devices** 142C - 146C have uninterrupted access to commands and data in the multimedia memory 160 while...

...commands and data to the multimedia memory 160.

Figure 19 - High Speed Memory Channel Per **Peripheral**

Referring now to Figure 19, a computer system is shown which includes a PCI or multimedia bus 120 and which also includes a separate memory data channel for each **peripheral** **connected** to the bus 120. The computer system of Figure 19 is similar to the computer...

...However, the computer system of Figure 19 includes a separate memory

data channel for each **peripheral** to the memory controller. As described below, multimedia **devices** use the respective memory data channel 130 for high speed data transfers. In the following...

...convenience.

As shown, the computer system includes a central processing unit (CPU) 102 which is **coupled** through a CPU local bus 104 to a host/PCI/cache bridge or chipset 106. The chipset 106 includes various bridge logic, **peripheral** logic and arbitration logic 107, as described above with reference to Figure 1. As shown...

...includes PCI bridge logic 932 and a memory controller 934. The bridge or chipset 106 **couples** through a memory bus 108 to main memory 110. The main memory 110 is preferably...

...or other types of memory, as desired. The memory controller 934 in the chipset 106 **interfaces** to the main memory 110.

The host/PCI/cache bridge or chipset 106 **interfaces** to a local expansion bus or system bus 120. In the preferred embodiment, the local expansion bus 120 is the **peripheral** **component** interconnect (PCI) bus 120 or other type of system bus such as a dedicated multimedia or **real** - **time** **bus** . Various types of **devices** may be **connected** to the PCI bus 120. Expansion bus bridge logic I and an expansion bus (both not shown) may also be **coupled** to the PCI bus 120, as described above.

One or more multimedia **devices** or multimedia **devices** 902-910 are **coupled** to the PCI bus 120. In the embodiment shown, a CD-ROM 902, a Video...

...Audio card 906, a telephony card 908, and an MPEG decoder card 910 may be **coupled** to the PCI bus 120. Various other types of **peripherals** may be **connected** to the bus 120, as desired.

Each of the multimedia **devices** 902 - 910 includes a dedicated memory data channel 912 - 920, respectively, which **connects** to the memory controller 934 in the chipset logic 106. Each of the memory data...

...or a 4 bit, 8 bit bus, or 16 bit bus. Each of the multimedia **devices** 902 - 910 uses its dedicated memory data channel 912- 920 to perform data accesses and...

...bypassing PCI bus arbitration and PCI bus cycles. The dedicated memory channels may also be **coupled** directly to the main memory 110 instead of to the memory controller 934.

The multimedia **devices** 902 - 910 each include bus **interface** circuitry 940 which includes standard PCI **interface** circuitry for communicating on the PCI bus 120. The **interface** circuitry 940 in each of the multimedia **devices** 902 - 910 also includes **interface** logic for **interfacing** to the respective dedicated memory data channel 912 - 920. The multimedia **devices** 902 - 910 use the PCI bus 120 to communicate data between the respective **devices** , and each uses its respective channel for main memory accesses.

The multimedia **devices** 902 - 910 may be any of various types of input/output **devices** , including multimedia **devices** and communication **devices** , as described above. The multimedia **devices** 902 - 910 are preferably similar to the multimedia **devices** 902 - 910 described above, except that the **interface** logic in the multimedia **devices** 902 - 910 each include memory data channel **interface** logic, as described below. As described above, the multimedia **devices** 902 - 910 may comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards, network **interface** cards, SCSI adapters for

interfacing to various input/output **devices** , such as CD-ROMS and tape drives, or other **devices** as desired.

Thus, the multimedia **devices** 902 - 910 communicate with each other via the PCI bus 120 and also communicate with...

...110 via the PCI bus 120, as is well known in the art.

The multimedia **devices** 902 - 910 also each communicate data to and from the main memory 110 using the **device** 's respective dedicated memory data channel. The multimedia **devices** 902 - 910 preferably each use its dedicated memory data channel for addressing, control, status and handshaking signals, as well as for data communications. Thus the **devices** 902 - 910 do not utilize any PCI bus cycles when communicating over their respective memory data channel. Altematively, the multimedia **devices** 902-910 set up the memory data channel transfer using PCI bus cycles and then perform the transfer on the data channel. Thus, in one embodiment, each multimedia **device** uses the PCI bus address and control signals to set up a date transfer on the respective memory data channel as discussed with reference to Figure 3A. A multimedia **device** may also use the PCI bus address and control signals to set up periodic transfers ...

...in a similar manner to that discussed above with respect to Figure 3d, once the **device** has set up the periodic transfer, the memory 110 periodically transfers data to the multimedia **devices** , or vice versa, at periodic intervals.

In the embodiment of Figure 19, arbitration logic 936 is comprised in the chipset 106 and/or in the memory controller 934 and **coupled** to the memory controller 934. The arbitration logic 936 receives memory requests from each of the **devices** 902-910 and performs arbitration for the **devices** 902 - 910 attempting to access the main memory 110. In this embodiment, the multimedia **devices** 902 - 910 provide request signals on their respective channel to the arbitration logic 936, and...

...transfers from the main memory 110 to the respective memory data channels.

Figure 20 - Multimedia **Devices**

Referring now to Figure 20, a block diagram is shown illustrating one of the multimedia **devices** 902-910, such as multimedia **device** 902. As shown. the multimedia **device** 902 includes **interface** logic 940 comprising PCI **interface** circuitry 942 for communicating on the PCI bus 120, and also including memory data channel **interface** logic 944 for **interfacing** to the respective data channel. The multimedia **device** 902 also may include a digital signal processor (DSP) 210 or other **hardware** circuitry for implementing a multimedia or communications function. Each of the multimedia **devices** 902 - 910 preferably includes the **interface** logic 940, as shown in Figure 20.

The multimedia **devices** 902 - 910 preferably use their respective memory data **channel** only for high speed data transfers of **real - time** stream data information and/or **periodic** data transfers to or from the main memory 110. In an alternate embodiment, the memory data channels are used by each multimedia **device** for any of various types of multimedia or communications data transfers to or from main...

...data channel includes only data lines, such as an 8 bit or 16 bit data **path** , and does not include address or control **portions** . In this embodiment of the invention, as mentioned above, each of the multimedia **devices** 902 - 910 uses the PCI bus 120 for addressing and control for transfers on the respective memory data **channel** .

Figure. 21 - **PCI Bus** Including a **Real - Time** Mode

Referring now to Figure 21, a computer system is shown which includes an expansion...

...real-time /multimedia mode optimized for multimedia transfers of periodic data. As described below, multimedia **devices** use ... convenience.

As shown, the computer system includes a central processing unit (CPU) 102 which is **coupled** through a CPU local bus 104 to a host/PCI/cache bridge or chipset 106...

...mode logic 960 according to the present invention for selectively and dynamically placing the expansion **bus** 120 in either a normal mode or a real time mode **according** to the present invention.

The bridge or chipset 106 **couples** through a memory bus 108 to main memory 110. The main memory 110 is preferably...

...types of memory, as desired. The chipset logic 106 preferably includes a memory controller for **interfacing** to the main memory 110.

The host/PCI/cache bridge or chipset 106 **interfaces** to a local expansion bus or system bus 120. In the preferred embodiment, the local expansion bus 120 is the **peripheral component** interconnect (PCI) bus 120. However, it is noted that other local buses may be used, such as the VESA (Video Electronics Standards Association) VL bus or "Firewire". Various types of **devices** may be **connected** to the PCI bus 120. Expansion bus bridge logic 150 and an expansion bus 152 may also be **coupled** to the PCI bus 120, as described above. As mentioned above, the mode logic 960...

...to place the PCI bus 120 in either a normal PCI mode or in a **real - time** /multimedia mode optimized for multimedia transfers of periodic data.

The computer system shown in Figure 21 optionally includes a real-time **bus** , also referred to as a multimedia **bus** 130 (not shown in Figure 21). The multimedia bus 130 preferably includes a 32 or 64 bit data **path** and may include address and control **portions** . The computer system shown in Figure 21 may include a dedicated control channel, such as...

...bus 120 when the PCI bus 120 is in multimedia mode.

One or more multimedia **devices** or multimedia **devices** 142D, 144D, and 146D are **coupled** to each of the PCI bus 120 and the multimedia bus 130. As shown in Figure 22, the multimedia **devices** 142D - 146D each include bus **interface** circuitry 962 which includes standard PCI **interface** circuitry 964 for **interfacing** to the PCI bus 120 when the PCI bus is in a normal PCI mode. The bus **interface** circuitry 962 also includes **interface** logic 966 for **interfacing** to the PCI bus 120 when the PCI bus 120 is in the multimedia mode. The bus **interface** circuitry 962 also includes **interface** logic 968 for **interfacing** to the optional multimedia bus 130.

The multimedia **devices** 142D - 146D may be any of various types of input/output **devices** , including multimedia **devices** and communication **devices** . as described above. The multimedia **devices** 142D - 146D are preferably similar to the multimedia **devices** 142 - 146 described above, except that the **interface** logic 962 in the multimedia **devices** 142D - 146D each include the **interface** logic for **interfacing** to the PCI bus 120 in **multiple** modes. As described above, the multimedia **devices** 142D - 146D may comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards, network **interface** cards, SCSI adapters for **interfacing** to various input/output **devices** , such as CD-ROMS and tape drives, or other **devices** as desired.

Thus, the multimedia **devices** 142D - 146D communicate with each other and with the CPU 102 and main memory 110 via the PCI bus 120, as is well known in the art. The multimedia **devices** 142D - 146D also communicate data between using the PCI bus signal lines 120 when the PCI bus 120 is in the multimedia mode. As noted above, the real-time **bus** or multimedia **bus** 130 is optionally used to supplement the PCI bus 120 when the PCI bus 120...

...comprises placing the system bus or PCI bus 120 in a special mode optimized for **real - time** data transfers. In one embodiment of Figure 21, the special mode comprises a byte sliced...

...11 and 12. In another embodiment, the special or real time mode comprises placing the **PCI bus** 120 in mode for performing periodic multimedia data transfers as described above. Other types of...

...which increases the performance of real-time applications. The computer system includes a PCI local **bus** and a real-time or multimedia **bus** . The multimedia **bus** may be used only for periodic data, and either the PCI bus or a separate in the various **peripheral devices** which provide for time slotting and improved data transfer performance.

Although the system and method of the present invention has been described in **connection** with the preferred embodiment, it is not intended to be limited to the specific form...

...as can be reasonably included within the scope of the invention as defined by the **appended** claims.

```
Set     Items   Description
S1    1390918   DIVID? OR DIVY? OR ALLOCAT? OR ALLOT? OR DIVVY? OR RATION?
S2    1265401   APPORTION? OR DESIGNAT? OR ASSIGN? OR EARMARK? OR DISPENS?
            OR SHARE?
S3     657399   METE? OR PARCEL?()OUT OR DOLE? OR DELEGAT? OR RELEGAT? OR -
            PRORAT? OR PRO()(RATA? OR RATE?)
S4    7696247   DISTRIBUT? OR CORRELAT? OR COLLOCAT? OR CONSIGN? OR ROUTE?
S5    3067592   PARTITION? OR SEGMENT? OR PORTION? OR SECTION? OR SUBBUS? -
            OR SUB()(BUS OR BUSES)
S6    4023870   DYNAMIC? OR ON(2W)FLY OR REALTIME? OR REAL()TIME? OR WHEN(-
            )NEEDED OR CHANGABL? OR CHANGEABL?
S7      63205   HOTSWAP? OR HOT()SWAP? OR AS()NEEDED? OR CASE(2W)CASE()BAS-
            IS? OR CUSTOMIZ? OR CUSTOMIS?
S8    1465324   (CUSTOM? OR TAILOR?)()(MAKE? OR MAKING? OR MADE?) OR CONTI-
            NUOUS? OR CONSTANTLY?
S9     136576   BUS OR BUSSES
S10     90360   PCI? ? OR ISA? ? OR EISA? ? OR VLBUS? OR AGP? ? OR USB? ? -
            OR MCA? ? OR VESABUS? OR VESALOCAL?
S11   1250223   CONNECTOR? OR PIN? ? OR CONDUCTOR? OR WIRE? OR (ELECTRIC? -
            OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(PATH? OR VIA? ?
             OR CONNECTION?) OR DATA()TRANSMITTER?
S12    139987   (ELECTRIC? OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(-
            TRACK? OR LANE? OR CHANNEL? OR PORT? OR INTERCONNECT?)
S13     49318   S1:S5 AND S6:S8 AND S9:S12
S14      7467   ACCORDING? OR DEPENDING? OR PER OR ONE(2W)ONE OR CORRESPON-
            D?
S15      8143   MATCH? OR CONFORM? OR COINCID? OR CONSISTEN? OR SIMILAR? OR
             SYNCHRON?
S16      2952   EQUAL? OR PROPORTION? OR CONTINGEN? OR HING? OR PREDICAT? -
            OR RELEGAT?
S17      2176   RELY? OR RELIAN? OR COMMENSURAT? OR EQUIVAL? OR COMPARABL?
            OR EQUIVAL?
S18      2677   COMPATIB? OR HOMOLOG? OR SYMMET? OR SYNONYM? OR HOMOGEN? OR
             EVENLY?
S19     12322   NUMBER? OR VOLUME? OR QUANTIT? OR AMOUNT? OR HOW()MANY
S20      8415   MAGNITUD? OR QUOTA? OR ASSEMBLAG? OR SIZE? OR TOTAL? OR AC-
            CUMULATION?
S21     16478   ABUNDAN? OR DIMENSION? OR WORKLOAD? OR BANDWIDTH? OR PLURA-
            L? OR MULTIP? OR MULTIT?
S22     13650   ATTACH? OR CONNECT? OR LINK? OR INSTALL? OR PLUG?()IN OR A-
            PPEND? OR CONFIGUR?
S23      6848   COUPL? OR AFFIX? OR HOOK?()UP OR NETWORKED? OR YOKE? OR IN-
            TERFAC?
S24      8863   DEVICE? OR HARDWARE? OR APPLIANC? OR APPARAT? OR ATTACHMEN-
            T? OR MODULE?
S25      4807   COMPONENT? OR PERIPHERAL? OR PDA? ? OR PALMPILOT? OR PALM(-
            )PILOT? OR ELECTRONIC()PC
S26        99   (PORTABL? OR MOBIL? OR HANDHELD? OR HAND()HELD? OR ELECTRO-
            NIC? OR PALMTOP? OR PALM()TOP)()(UNIT? ? OR ORGANIZER?)
S27      5093   S13 AND S6:S8(7N)S1:S5(7N)S9:S12
S28       332   S27 AND S14:S23(10N)S24:S26
S29       247   S28 AND PY<2003
S30       183   RD (unique items)
S31        69   S30 AND S14:S18 AND S19:S23 AND S22:S26
S32        69   RD (unique items)
File   2:INSPEC 1969-2005/Oct W1
         (c) 2005 Institution of Electrical Engineers
```

File 6:NTIS 1964-2005/Oct W1
(c) 2005 NTIS, Intl Cpyrght All Rights Res
File 8:Ei Compendex(R) 1970-2005/Oct W1
(c) 2005 Elsevier Eng. Info. Inc.
File 34:SciSearch(R) Cited Ref Sci 1990-2005/Oct W1
(c) 2005 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2005/Sep
(c) 2005 ProQuest Info&Learning
File 62:SPIN(R) 1975-2005/Aug W1
(c) 2005 American Institute of Physics
File 65:Inside Conferences 1993-2005/Oct W2
(c) 2005 BLDSC all rts. reserv.
File 94:JICST-EPlus 1985-2005/Aug W2
(c)2005 Japan Science and Tech Corp(JST)
File 95:TEME-Technology & Management 1989-2005/Sep W1
(c) 2005 FIZ TECHNIK
File 99:Wilson Appl. Sci & Tech Abs 1983-2005/Sep
(c) 2005 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2005/Oct 10
(c) 2005 The Gale Group
File 144:Pascal 1973-2005/Oct W1
(c) 2005 INIST/CNRS
File 239:Mathsci 1940-2005/Nov
(c) 2005 American Mathematical Society
File 256:TecInfoSource 82-2005/Nov
(c) 2005 Info.Sources Inc
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info

32/3,K/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

04766274 INSPEC Abstract Number: C91003612
Title: A dynamically segmented bus **architecture**
Author(s): Xu BaiQiang; Ida, N.
Author Affiliation: Dept. of Electr. Eng., Akron Univ., OH, USA
Journal: Computers & Electrical Engineering vol.16, no.3 p.139-58
Publication Date: 1990 Country of Publication: USA
CODEN: CPEEBQ ISSN: 0045-7906
U.S. Copyright Clearance Center Code: 0045-7906/90/$3.00+0.00
Language: English
Subfile: C

Title: A dynamically segmented bus **architecture**
Abstract: Presents a **dynamically segmented bus** (DS- **Bus**) architecture for disturbed systems as an alternative to existing architectures, such as multi- **bus** , multi-stage network, or hypercube **connection** . Design considerations of the DS- **Bus** arbiter, as the key **component** on the DS- **Bus** , are discussed. A specific design of the arbiter is given with a resolution time **proportional** to the **number** of grants. Analysis of DS- **Bus** contention is carried out by analytic methods and by simulation. Formulas are derived for parameters such as accept rate, capacity, inter-communication delay, and **bandwidth** of the DS- **Bus** . As with other architectures, the performance of the DS- **Bus** is application sensitive. It is shown, by comparison, that the DS- **Bus** architecture is a good approach to organize a large scale parallel computing machine. Finally, a large scale DS- **Bus** system design is proposed.
Descriptors: computer **interfaces** ;
Identifiers: **bus** contention...

... **bus** architecture...

... **dynamically segmented bus** architecture...

...DS- **Bus** arbiter...

... **bandwidth** ;
1990

32/3,K/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

04985359 INSPEC Abstract Number: C91064199
Title: Futurebus+ arbitration
Author(s): Hawley, D.
Author Affiliation: Nat. Semicond. Corp., Santa Clara, CA, USA
Conference Title: Wescon/89. Conference Record p.596-601
Publisher: Electron. Conventions Manage, Ventura, CA, USA
Publication Date: 1989 Country of Publication: USA v+787 pp.
Conference Sponsor: IEEE; ERA
Conference Date: 14-15 Nov. 1989 Conference Location: San Francisco, CA, USA
Language: English
Subfile: C

Abstract: The new Futurebus+ arbitration protocol provides a large **number** of priority levels for accurate **real - time** task scheduling, and a fairness protocol that allows an even **allocation** of **bus bandwidth** to **multiple modules** . This arbitration takes place on its own independent set of lines in parallel with data transfers. The article discusses: the **allocation** protocol w.c.t. priority fairness and uniqueness; arbitration competition including competition **number** and parallel contention mechanism; control signals for arbitration **synchronisation** and arbitration condition; and control acquisition sequence. The Futurebus+ arbitration mechanism also provides a **number** of other facilities, including error detection and recovery, parking, **bus** master identification, emergency messages, and board **synchronization** during reset and live insertion or withdrawal of **modules** . These are briefly mentioned.
Descriptors: computer **interfaces** ;
...Identifiers: **real - time** task scheduling...

... **bus bandwidth** ; ...

... **multiple modules** ; ...

...competition **number** ; ...

...arbitration **synchronisation** ;
1989

32/3,K/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

07912770 INSPEC Abstract Number: C2001-06-6150N-030
Title: A distributed **asynchronous execution semantics for programming the middleware machine**
Author(s): Berry, A.; Kaplan, S.
Author Affiliation: Dept. of Comput. Sci. & Electr. Eng., Queensland Univ., Brisbane, Qld., Australia
Conference Title: Proceedings 5th International Symposium on Autonomous Decentralized Systems p.187-95
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 2001 Country of Publication: USA xvi+484 pp.
ISBN: 0 7695 1065 5 Material Identity Number: XX-2001-00562
U.S. Copyright Clearance Center Code: 0 7695 1065 5/2001/$10.00
Conference Title: Proceedings of 5th International Symposium on Autonomous Decentralized Systems
Conference Sponsor: IEEE Comput. Soc.; Inf. Process. Soc. Japan; Soc. Instrument & Control Eng. Japan; IEICE of Japan; IFIP; IFAC; OMG; TINA-C; Manuf. Sci. & Technol. Center, Japan
Conference Date: 26-28 March 2001 Conference Location: Dallas, TX, USA
Language: English
Subfile: C

Title: A distributed **asynchronous execution semantics for programming the middleware machine**
Abstract: **Distributed** software is traditionally built by **connecting** a set of software **components** using a communications abstraction. The interaction semantics provided by the abstraction is predominantly static: any programming of behavior occurs in the **components** or in local wrappers around those **components** . While autonomous behavior can be programmed over these abstractions, there is increasing awareness that static interaction models are not sufficient to capture the semantic diversity found in **dynamic** , evolving **distributed** systems. This paper presents an asynchronous, **distributed** and executable semantic model suitable for implementing programmable **connector** objects. Programs described using the semantic model can be jointly executed by a set of autonomous, **distributed** participants with no explicit **synchronization** of execution state. By removing the requirement for explicit **synchronization** , participants can execute independently with no requirement for centralized mediation, and the asynchrony of the model implicitly allows for potentially high latencies in **distributed** environments like the Internet. This combination of properties makes the model ideal for e-commerce...
...Descriptors: **distributed** programming
Identifiers: **distributed** asynchronous execution semantics...

... **distributed** software...

...programmable **connector** objects
2001

32/3,K/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

07684003 INSPEC Abstract Number: B2000-10-7210B-004, C2000-10-7410H-007
Title: The design of distributed **measurement systems based on IEEE1451 standards and** distributed **time services**
Author(s): Burch, J.; Eidson, J.; Hamilton, B.
Author Affiliation: Agilent Technol. Inc., Palo Alto, CA, USA
Conference Title: Proceedings of the 17th IEEE Instrumentation and Measurement Technology Conference [Cat. No. 00CH37066] Part vol.2 p. 529-34 vol.2
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 3 vol. (xliv+1615) pp.
ISBN: 0 7803 5890 2 Material Identity Number: XX-2000-01324
U.S. Copyright Clearance Center Code: 0 7803 5890 2/2000/$10.00
Conference Title: 17th IEEE Instrumentation and Measurement Technology Conference
Conference Sponsor: IEEE Instrum. & Meas. Soc.; Baltimore Sect. IEEE; Washington Sect. I&M Soc. Chapter
Conference Date: 1-4 May 2000 Conference Location: Baltimore, MD, USA
Language: English
Subfile: B C

Title: The design of distributed **measurement systems based on IEEE1451 standards and** distributed **time services**
Abstract: This paper discusses the design challenges in creating effective and robust **distributed** measurement and control systems. The design of **distributed** measurement systems is greatly facilitated by recent standards such as IEEE1451.1 and IEEE1451.2, and the existence of network infrastructure features such as **distributed** time services. The point-to-point **connection** between the central controller and a **peripheral** is usually accomplished via a serial protocol such as RS-232, HART/sup TM/, or a specialized **bus** such as IEEE488. A **distributed** design allows additional degrees of freedom to meet **real - time** requirements and an opportunity to build more flexible yet more robust systems. A variety of...

... Another approach is to use services built on a global sense of time established by **synchronizing real - time** clocks contained in each **component** . These services are discussed both theoretically and in terms of an example system. To illustrate these points, a simple **distributed** measurement system is examined both in terms of the design issues and the performance. This system has been constructed out of a mixture of commercially available and prototype **components** that make use of Ethernet, the IEEE1451 standards, **synchronized** clocks, and commonly available commercial infrastructure services and **components** such as Web browsers, databases and other common application tools.
...Descriptors: **distributed** control...

...network **interfaces**
Identifiers: **distributed** measurement systems...

... **distributed** time services...

... **peripheral** instruments...

... **real time** programming...

...point-to-point **connection** ; ...

... **distributed** design...

... **real - time** clocks...

... **synchronized** clocks...

...clint-server **interface** ; ...
...publish-subscribe **interface**

```
Set     Items   Description
S1    6847462   DIVID? OR DIVY? OR ALLOCAT? OR ALLOT? OR DIVVY? OR RATION?
S2    3561499   APPORTION? OR DESIGNAT? OR ASSIGN? OR EARMARK? OR DISPENS?
S3   18427491   SHARE? OR SHARING?
S4    2631747   METE? OR PARCEL?()OUT OR DOLE? OR DELEGAT? OR RELEGAT? OR -
           PRORAT? OR PRO()(RATA? OR RATE?)
S5   13781281   DISTRIBUT? OR CORRELAT? OR COLLOCAT? OR CONSIGN? OR ROUTE?
S6    8669299   PARTITION? OR SEGMENT? OR PORTION? OR SECTION? OR SUBBUS? -
           OR SUB()(BUS OR BUSES)
S7    4066442   DYNAMIC? OR ON(2W)FLY OR REALTIME? OR REAL()TIME? OR WHEN(-
           )NEEDED OR CHANGABL? OR CHANGEABL?
S8    1944884   HOTSWAP? OR HOT()SWAP? OR AS()NEEDED? OR CASE(2W)CASE()BAS-
           IS? OR CUSTOMIZ? OR CUSTOMIS?
S9    2337403   (CUSTOM? OR TAILOR?)()(MAKE? OR MAKING? OR MADE?) OR CONTI-
           NUOUS? OR CONSTANTLY?
S10    381904   S7:S9(7N)S1:S6
S11    105217   BUS OR BUSSES
S12     10339   PCI? ? OR ISA? ? OR EISA? ? OR VLBUS? OR AGP? ? OR USB? ? -
           OR MCA? ? OR VESABUS? OR VESALOCAL?
S13    132441   CONNECTOR? OR PIN? ? OR CONDUCTOR? OR WIRE? OR (ELECTRIC? -
           OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(PATH? OR VIA? ?
            OR CONNECTION?) OR DATA()TRANSMITTER?
S14     12810   (ELECTRIC? OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(-
           TRACK? OR LANE? OR CHANNEL? OR PORT? OR INTERCONNECT?)
S15    184513   ACCORDING? OR DEPENDING? OR PER OR ONE(2W)ONE OR CORRESPON-
           D?
S16    136082   MATCH? OR CONFORM? OR COINCID? OR CONSISTEN? OR SIMILAR? OR
            SYNCHRON?
S17     54889   EQUAL? OR PROPORTION? OR CONTINGEN? OR HING? OR PREDICAT? -
           OR RELEGAT?
S18     68738   RELY? OR RELIAN? OR COMMENSURAT? OR EQUIVAL? OR COMPARABL?
           OR EQUIVAL?
S19     45472   COMPATIB? OR HOMOLOG? OR SYMMET? OR SYNONYM? OR HOMOGEN? OR
            EVENLY?
S20    192697   NUMBER? OR VOLUME? OR QUANTIT? OR AMOUNT? OR HOW()MANY
S21    148236   MAGNITUD? OR QUOTA? OR ASSEMBLAG? OR SIZE? OR TOTAL? OR AC-
           CUMULATION?
S22    138545   ABUNDAN? OR DIMENSION? OR WORKLOAD? OR BANDWIDTH? OR PLURA-
           L? OR MULTIP? OR MULTIT?
S23    202320   ATTACH? OR CONNECT? OR LINK? OR INSTALL? OR PLUG?()IN OR A-
           PPEND? OR CONFIGUR?
S24    103127   COUPL? OR AFFIX? OR HOOK?()UP OR NETWORKED? OR YOKE? OR IN-
           TERFAC?
S25    134227   DEVICE? OR HARDWARE? OR APPLIANC? OR APPARAT? OR ATTACHMEN-
           T? OR MODULE?
S26     97777   COMPONENT? OR PERIPHERAL? OR PDA? ? OR PALMPILOT? OR PALM(-
           )PILOT? OR ELECTRONIC()PC
S27      1111   (PORTABL? OR MOBIL? OR HANDHELD? OR HAND()HELD? OR ELECTRO-
           NIC? OR PALMTOP? OR PALM()TOP)()(UNIT? ? OR ORGANIZER?)
S28     34665   S10 AND S1:S9(7N)S11:S14
S29     10654   S28 AND S7:S9(5N)S1:S6(5N)S11:S14
S30       320   S29 AND (S1:S6 OR S11:S14)(5N)S15:S19(5N)S20:S22(10N)S23:S-
           27
S31       154   S30 AND S23:S24(7N)S25:S27
S32       128   S31 AND PY<2003
S33        83   RD (unique items)
File   9:Business & Industry(R) Jul/1994-2005/Oct 11
         (c) 2005  The Gale Group
File  13:BAMP 2005/Oct W1
         (c) 2005  The Gale Group
File  15:ABI/Inform(R) 1971-2005/Oct 12
```

(c) 2005 ProQuest Info&Learning
File 16:Gale Group PROMT(R) 1990-2005/Oct 11
(c) 2005 The Gale Group
File 20:Dialog Global Reporter 1997-2005/Oct 12
(c) 2005 Dialog
File 47:Gale Group Magazine DB(TM) 1959-2005/Oct 12
(c) 2005 The Gale group
File 75:TGG Management Contents(R) 86-2005/Oct W1
(c) 2005 The Gale Group
File 88:Gale Group Business A.R.T.S. 1976-2005/Oct 12
(c) 2005 The Gale Group
File 98:General Sci Abs/Full-Text 1984-2004/Dec
(c) 2005 The HW Wilson Co.
File 141:Readers Guide 1983-2004/Dec
(c) 2005 The HW Wilson Co
File 148:Gale Group Trade & Industry DB 1976-2005/Oct 12
(c)2005 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2005/Oct 11
(c) 2005 The Gale Group
File 369:New Scientist 1994-2005/Jul W1
(c) 2005 Reed Business Information Ltd.
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 484:Periodical Abs Plustext 1986-2005/Oct W2
(c) 2005 ProQuest
File 553:Wilson Bus. Abs. FullText 1982-2004/Dec
(c) 2005 The HW Wilson Co
File 610:Business Wire 1999-2005/Oct 12
(c) 2005 Business Wire.
File 613:PR Newswire 1999-2005/Oct 12
(c) 2005 PR Newswire Association Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2005/Oct 12
(c) 2005 The Gale Group
File 624:McGraw-Hill Publications 1985-2005/Oct 12
(c) 2005 McGraw-Hill Co. Inc
File 634:San Jose Mercury Jun 1985-2005/Oct 11
(c) 2005 San Jose Mercury News
File 635:Business Dateline(R) 1985-2005/Oct 12
(c) 2005 ProQuest Info&Learning
File 636:Gale Group Newsletter DB(TM) 1987-2005/Oct 11
(c) 2005 The Gale Group
File 647:CMP Computer Fulltext 1988-2005/Sep W4
(c) 2005 CMP Media, LLC
File 674:Computer News Fulltext 1989-2005/Oct W2
(c) 2005 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2005/Oct 12
(c) 2005 Dialog
File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc

33/3,K/6 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01786134 04-37125
An in-depth look at server clustering
Elizer, Lee H; Swift, David G
Computer Technology Review PP: 40-44 Fourth Quarter 1998
ISSN: 0278-9647 JRNL CODE: CTN
WORD COUNT: 1926

...TEXT: on the software vendor and the clustering architecture being used. The issue of how much **hardware** can be **shared** versus how much hardware needs to be duplicated and **how many** nodes **per** cluster are supported must be addressed. **Hardware connectivity** is very dependent upon the clustering architecture of individual vendors.

Clustering software must provide cluster...Additionally, most PC servers with "dual-peer PCI" buses will have a secondary bus with **ISA** or **EISA** slots and an embedded **real - time** clock. This clock watches for interrupts, such as the keyboard, all of which are 8MHz...

...the clustering solution exposed to an additional point of failure.

I/O bottlenecks are a **continuous** problem. Load balancing reduces the occurrence of I/O bottlenecks by **allocating** I/O on a **dynamic** basis to the least used host **bus** adapter. Users need to be sure that the clustering solution being considered has been tested...

33/3,K/30 (Item 16 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

05424623 Supplier Number: 48227456 (USE FORMAT 7 FOR FULLTEXT)
Standard Microsystems Launches New PC Connectivity Product Line.
Business Wire, p01151297
Jan 15, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 896

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...the first in a new family of integrated circuit (IC) products designed to provide advanced **connectivity** features among next-generation PCs and PC **peripherals** . Products planned for this new line include IC's supporting emerging industry standards, such as...

With today's announcement, SMSC introduced the industry's first bandwidth-efficient, multiple-endpoint **USB** **peripheral** controller IC. The USB97C100, which **connects** **ISA** -type **peripherals** to the Universal Serial **Bus** , is aimed at fully utilizing the **USB** bandwidth in PC **peripheral** applications. With two addresses and up to 16 transmit and 16 receive endpoints **per** address, the USB97C100 can simultaneously **attach** several **peripherals** to a single USB **connection** . This new IC supports a wide range of **peripherals** , including PC serial ports, parallel ports, floppy disk controllers, Ethernet controllers, PC keyboards and mice.

In order to place multiple **devices** on a single USB **connection** without loss of performance, a **peripheral** controller must use the available bandwidth effectively. The USB97C100 does this through Standard Microsystems' patented dynamic memory management architecture, originally developed for the Company's Ethernet controllers. Unlike other **USB** peripheral controllers, the USB97C100 **dynamically** **allocates** data buffers from a 4K-byte internal memory. The chip's hardware determines the specific...

...8051 MCU, external 1MB memory interface, an 8237 ISA DMA controller, and a quasi-ISA **peripheral** **interface** with 64KB I/O and separate 1MB memory space in a 128-pin QFP package...
...for the packet-oriented nature of the Universal Serial Bus. The USB97C100 is the first **USB** controller that can **continuously** sustain the theoretical maximum bandwidth of the Universal Serial Bus on back-to-back frames...

...such as video, audio, and data acquisition, as well as for porting multiple PC legacy **peripherals** to a single USB **connection** ."

Standard Microsystems provides a complete development environment for the USB97C100, consisting of an evaluation/software...
19980115

33/3,K/32 (Item 18 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03105373 Supplier Number: 44232684 (USE FORMAT 7 FOR FULLTEXT)
A Guide to Multislot-Hub Vital Parts
CommunicationsWeek, p55
Nov 15, 1993
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 764

... a chassis slot and then plugs into the backplane via one or more on-board **connectors** . Users may note that **modules** for different transmission technologies have **connectors** in different locations. They are set up this way because different transmission technologies are handled ...

...be used. For such a switch-over to occur automatically or via software, the hub **modules** need to **connect** to both backplane regions concurrently.
A bus is a specific traffic-carrying path within the...

...however, varies widely among products.
In most cases there are at least two buses that **link** all the **modules** in a concentrator. One is used for carrying user data between modules, while a separate management bus is often used to exchange administrative, control and status messages between the **interface modules** and one or more control or management modules.
While a bus is a physical electrical...

...32 or 64 - carry two or more bytes concurrently.
Throughput, however, differs from this raw **bandwidth** . Since throughput represents the user data traffic-carrying capacity of a **bus** , it varies **according** to access and contention schemes that are used to control how **multiple modules share** a **bus** ' **bandwidth** . .
Three prevalent forms of access control are time-division multiplexing (TDM), which assigns a fixed amount of bandwidth to each **module** ; arbitrated access, which relies on an arbitration protocol to **dynamically assign** bandwidth; and collision-based access, which operates the **bus** like a thin- or thick-wire Ethernet LAN. These different access methods are used to...

...call for the setup of temporary connections for high-speed blasts of traffic between communicating **modules** or **interfaces** . In most cases they are oriented toward meeting future asynchronous transfer mode traffic. If the...
...are also called channels or segments), two token-ring paths and one or two Fiber **Distributed Data** Interface (FDDI) **paths** .
These different types of LAN paths typically are carried on separate buses because different buses...

...separate, collision-based buses. Multiple token-ring channels are often carried within the same serial **bus** with channels **assigned** to different TDM time slots.
Some TDM buses are flexible enough so that the same...
19931115

33/3,K/70 (Item 1 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

04164053 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Windows 98, iMac fuel USB boom
Georgia, Bonny L
Home-Office Computing (GFHC), v17 n3, p16, p.1
Mar 1999
ISSN: 0899-7373 JOURNAL CODE: GFHC
DOCUMENT TYPE: News
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 322

1999

TEXT:
... slots on the back of your system may become front-runners.
When it comes to **hardware installations** , "USB's biggest promise is improved ease of use," says Steven Whalley, chairman of the...

...you swap, say, a mouse for a graphics tablet without powering down. Best of all, **peripherals** are recognized as soon as they're **connected** , without lengthy driver installations.
Two additional advantages are speed and expandability. USB transfers data up to 100 times faster than serial and 10 times faster than parallel **connections** , making short work of tasks such as downloading images from digital cameras. Moreover, dozens of **USB peripherals** can be daisy-chained, **sharing** a port and **bandwidth as needed** .
Although some Windows 95 systems had limited **USB** support, says Whalley, the **bus** 's current popularity is due to its **compatibility** with Windows 98 and Apple's iMac, both introduced last year. If you're upgrading ...

...to install and cost less than $40.
Whalley predicts that USB will soon become the **interface** of choice for **peripherals** , and serial and parallel ports will disappear. Already, the iMac offers only USB connections and...

33/3,K/79 (Item 6 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

00531238 CMP ACCESSION NUMBER: EET19930809S1525
Need for tolerance is paramount
LUIS F. MONTOYA
ELECTRONIC ENGINEERING TIMES, **1993** , n 758, 44
PUBLICATION DATE: 930809
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Power Technologies
WORD COUNT: 1427

, **1993**
... redundant system.

When an N+1 redundant system is implemented, an "excess" of power is **installed** . It is advisable to have the **total** load current **evenly distributed** among the **connected** power supplies instead of having some supplies delivering full power while others "work" almost idle...share method or independent current sharing. In essence, the power-supply designer provides a current- **share** **bus** that is used by the system designer to implement a fully redundant system with precise current **sharing** .

The concept behind the current- **share** **bus** is the implementation of a dictated bidirectional-current feedback network interconnected to the main control circuit inside each unit. This network senses the status of the **share** **bus** and adjusts the unit's output current accordingly. An enhanced description of this type of...

...and an almost unlimited number of paralleled modules without degradation of current-sharing accuracy.

The **share** signal is transmitted on a single-line **bus** that must be insensitive to noise pickup and parasitic elements. Another condition for this **share** **bus** is that the units must current- **share** when a signal is present, and they must continue to operate whether the bus is...

...compare the signal derived from the module's output current with that received from the **share** **bus** and adjust the unit's output (**as** **needed**) to drive this difference to zero. There are several techniques used to implement this circuit...

...accompanying figure shows a plot of the results obtained using PSpice simulation when two MST **modules** are **connected** in parallel. The plot shows the moment when, with one of the modules delivering all...

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